nature electronics

Article

https://doi.org/10.1038/s41928-025-01338-w

Solution-processed wafer-scale indium selenide semiconductor thin films with high mobilities

Received: 4 January 2024

Accepted: 2 January 2025

Published online: 03 February 2025

Check for updates

Jing He, Jifeng Ge, Junying Xue, Tingyi Xia, Yongping Dai, Shengqi Wang, Wenjie Li & Zhaoyang Lin

Solution-processed two-dimensional semiconductors could be used to create electronic devices on large scales and at low cost. However, the electronic performance of devices based on such materials is typically below that of devices based on materials grown via high-temperature chemical vapour deposition. Here we report the fabrication of indium selenide (InSe) semiconductor thin films using a colloidal solution of monolayer nanosheets (monolayer purity more than 98%). The InSe thin films are assembled on 4-inch wafers with conformal and intimate van der Waals contacts between the monolayer building blocks. We use the solution-processed films to fabricate InSe transistors that exhibit electron mobilities of 90–120 $cm^2 V^{-1} s^{-1}$, current on/off ratios of up to 10^7 and a small current hysteresis. We also show that InSe transistors with oxide encapsulation can remain stable in air for 3 months.

Solution-processable two-dimensional (2D) semiconductors could be used to fabricate flexible electronic and optoelectronic devices over large areas and at low cost[1–5]. Such materials, with low processing temperatures of below 300 °C, can be used to assemble high-quality 2D semiconductor thin films on a range of rigid and flexible substrates (including glass and plastic) through scalable solution-based deposition methods[2,5–11]. A variety of chemical methods have been developed to synthesize solution-processable 2D nanosheet inks, including bottom-up chemical synthesis and liquid-phase exfoliation assisted with high-power sonication or chemical intercalation[2,12–18]. By dispersing 2D nanosheets into selected solvents as colloidal solutions, stable and easy-to-handle ink materials can be formulated and used for film deposition and device fabrication[19]. An electrochemical molecular intercalation and exfoliation method that uses organic cation intercalants can, in particular, provide high-quality 2D semiconductor ink materials with well-preserved crystal structure and semiconducting characteristics[20–22].

The electrical performance of such solution-processed 2D semiconductors is, however, much lower than chemical vapour deposition (CVD)-grown crystals. For example, solution-processed n-type molybdenum disulfide (MoS_2) thin films fabricated with the electrochemical molecular intercalation and exfoliation method exhibit carrier mobilities of around 10 $cm^2 V^{-1} s^{-1}$ and on-/off-current ratios of around 10^6 on regular silicon dioxide (SiO_2) substrate[2]; tungsten diselenide (WSe_2) nanosheets obtained using a similar method can be switched to p-type with enhanced hole mobility of around 27 $cm^2 V^{-1} s^{-1}$ after bromine treatment[10]. With solution-processed MoS_2 thin films, carrier mobilities of up to around 80 $cm^2 V^{-1} s^{-1}$ have been reported by replacing the conventional SiO_2 and aluminium oxide (Al_2O_3) dielectrics with a specifically designed high-k layer (sodium-embedded alumina)[23]. In comparison, 2-inch monolayer MoS_2 thin film synthesized at 850–1,000 °C and 1-inch bilayer MoS_2 thin films synthesized at around 1,000 °C using a CVD approach have delivered average carrier mobilities of around 120 $cm^2 V^{-1} s^{-1}$ (up to 140 $cm^2 V^{-1} s^{-1}$) and around 107 $cm^2 V^{-1} s^{-1}$ (up to 122 $cm^2 V^{-1} s^{-1}$), respectively[24–26]. Recently, average mobilities of 120 $cm^2 V^{-1} s^{-1}$ (up to 190 $cm^2 V^{-1} s^{-1}$) have also been reported for CVD-grown 2-inch trilayer 3R-MoS_2 crystals[27]. The material quality and carrier mobility of these CVD-grown 2D semiconductors are higher than that of solution-processable films.

Department of Chemistry, Engineering Research Center of Advanced Rare Earth Materials (Ministry of Education), Tsinghua University, Beijing, China.
e-mail: zlin@mail.tsinghua.edu.cn

In pursuit of high-quality solution-processable 2D semiconductor thin films that can deliver electrical performance approaching the values offered with CVD-grown crystals, the 2D semiconductor indium selenide (InSe), which exhibits intrinsic mobility in the range of 300–1,000 $cm^2 V^{-1} s^{-1}$, is promising[28–33]. However, the solution-phase synthesis of InSe, and the subsequent fabrication of high-performance electronic devices, remains challenging. A key issue is developing a reliable solution-based method that can robustly produce high-quality 2D InSe semiconductors. InSe is not as chemically stable as MoS_2, especially in the form of thin monolayer or few-layer crystals[34,35], and thus the chemical synthesis of high-quality wafer-scale thin films through either CVD-based or solution-based methods is difficult. InSe thin films of 1 by 1 cm have been fabricated by pulsed laser deposition and used to create transistors that exhibit carrier mobilities of 0.6–10 $cm^2 V^{-1} s^{-1}$ and current on/off ratios of 10^2–10^5 (refs. 36,37). High-quality wafer-scale InSe thin films have also been fabricated via metal-organic CVD using dimethyl selenide and trimethylindium as precursors[38]. The InSe thin films, which were grown on a 2-inch Al_2O_3 substrate, exhibit a carrier mobility of around 4.5 $cm^2 V^{-1} s^{-1}$ and current on/off ratio of 10^4–10^5. These values are, however, still lower than the values reported on pristine thin flakes prepared by mechanical exfoliation. For solution-based methods, single InSe flakes produced from direct liquid-phase exfoliation have been shown to offer mobilities of 19 $cm^2 V^{-1} s^{-1}$ (ref. 8). Solution-PROCESSABLE InSe thin films with carrier mobilities of less than 0.1 $cm^2 V^{-1} s^{-1}$ (ref. 39) and around 5 $cm^2 V^{-1} s^{-1}$ (ref. 40) have also been reported (with film sizes of 4 by 4 mm).

In this Article, we report the fabrication of wafer-scale InSe semiconducting thin films using 2D monolayer inks (monolayer purity >98%). The ink material is formulated from a colloidal solution of 2D nanosheets obtained via an electrochemical molecular intercalation and exfoliation strategy. Using the high-purity 2D monolayer inks, we assemble InSe thin films on 4-inch wafers with tunable thicknesses, high uniformity (a film roughness around 2 nm) and preserved crystal structure integrity (suppressed material oxidation).

Within the assembled thin films, InSe monolayers stack with a conformal and clean van der Waals contact that resembles the pristine bulk layered crystal, which is a prerequisite for achieving high device performance. We use these materials to fabricate thin-film transistors with standard SiO_2 dielectrics and show that they offer an average electron mobility of around 90–120 $cm^2 V^{-1} s^{-1}$, a current on/off ratio of 10^7 and a small current hysteresis. With the help of ligand chemistry, we tune the carrier concentration in the film and obtain an improved subthreshold swing (SS) of around 1.8 V dec^{-1}. Our mobility values are comparable to the state-of-the-art performance obtained in CVD-grown wafer-scale MoS_2 semiconductor thin films[24–27]. The transistors also exhibit high device reproducibility and operational stability. For example, air-stable InSe transistors are created through oxide encapsulation, and the mobility and on/off ratio remain nearly unchanged after exposure to ambient air for 3 months.

Exfoliation of InSe monolayers in solution

The solution-processable high-purity InSe 2D monolayers were exfoliated following the protocol of electrochemical molecular intercalation of organic cations (for example, tetraheptylammonium bromide, THAB)[22]. Because InSe crystals, especially in the form of thin monolayers, are prone to oxidation by oxygen and moisture and thus are very sensitive to air[34,35]. Therefore, we have carried out the electrochemical intercalation and exfoliation process in an air-free environment (inside a nitrogen-filled glovebox with oxygen and water level <1 ppm), which is the key to high-quality 2D monolayers. Besides, both acetonitrile and dimethylformamide (DMF) were purged with nitrogen and dried with molecular sieve to remove the dissolved oxygen and residual moisture (oxygen and water level <1–10 ppm). By contrast, when intercalated in air with regular acetonitrile (for example, water level >200 ppm), the original dark brown InSe crystal turned yellow, which signifies the material oxidation caused by the oxygen and water in solvent (Fig. 1a,b and Supplementary Fig. 1). Previous reports suggest that InSe thin crystals can be readily oxidized to $InSe_{1-x}O_x$, Se and SeO_2, and thus InSe monolayers are vulnerable to the dissolved water and oxygen in organic solvents[35,41,42]. So, the colloidal solution of InSe nanosheets exfoliated in air appears bright yellow (inset photograph in Fig. 1b), in contrast to black pristine InSe crystals without oxidation. The transmission electron microscopy (TEM) image revealed many nanoparticle impurities caused by material oxidation (Fig. 1c and Supplementary Fig. 2a,b). The selected-area electron diffraction data show no diffraction spots, suggesting the destruction of InSe crystal lattice (inset in Fig. 1c). The oxidation of InSe to InO_x, Se and SeO_2 was also confirmed by X-ray photoelectron spectroscopy (XPS) analysis (Fig. 1d).

When in the air-free environment, the intercalated and exfoliated InSe crystal can maintain its original dark brown colour without turning yellow (Fig. 1e,f and Supplementary Fig. 1). No obvious nanoparticles or signs of material oxidation were observed in TEM images (Fig. 1g and Supplementary Fig. 2c,d). In particular, the six-fold symmetric electron diffraction pattern reveals the preserved InSe crystal structure of the exfoliated material (inset in Fig. 1g), in contrast to the sample prepared in air. Furthermore, XPS results confirm the preserved InSe structure with no oxidation peaks for InO_x, Se and SeO_2 (Fig. 1h and Supplementary Fig. 3). However, it does not fully exclude the possibility of a very low level of oxidation in the InSe that is beyond the detection limit of XPS. In this case, other advanced characterization techniques such as extended X-ray absorption fine structure may be required. The InSe crystal structure can be recovered after thermal annealing to decompose the surface molecules that, however, were not observed for the InSe exfoliated in air condition (Fig. 1i). The electrical measurement suggests that the InSe nanosheets exfoliated in air are not conductive ascribing to the material oxidation and structural damage (Fig. 1j and Supplementary Fig. 4). By contrast, the InSe nanosheets exfoliated in the nitrogen environment display the expected n-type semiconducting characteristics with an on/off ratio of roughly 10^7.

The large-area atomic force microscopy (AFM) image reveals a uniform thickness among about 100 exfoliated nanosheets (Fig. 1k and Supplementary Fig. 5). An individual nanosheet exhibits a thickness of ~1.7 nm (Supplementary Fig. 6). The statistical analysis of the thickness measured by AFM shows a narrow distribution with a high monolayer purity of >98% (Fig. 1l). Also, the lateral size of the exfoliated InSe nanosheets can be tuned from ~2 to ~0.5 μm simply by adjusting the sonication time (Supplementary Fig. 7). The nanosheets dispersion in DMF is stable for several days without obvious change in colour and optical absorption spectrum (Supplementary Fig. 8). As typically observed in previous In_2Se_3 monolayers[43], these exfoliated nanosheets are InSe monolayer crystals (monolayer thickness ~0.8 nm) capped with organic layers of ammonium molecules (molecular thickness ~0.9 nm), which together result in the larger apparent thickness. In the following sections, more experimental evidence for the monolayer nature from X-ray diffraction (XRD) and TEM analysis of the exfoliated InSe nanosheets will be discussed.

Solution-processed assembly of InSe thin films from monolayer ink

High-quality InSe thin films can be assembled on versatile substrates using a facile yet robust spin coating approach with high-purity 2D InSe monolayer ink materials. As a proof of concept, we have assembled a 4-inch InSe thin film on the silicon wafer. The wafer-scale thin film exhibits a uniform thickness suggested by the consistent colour across the substrate (Fig. 2a). The thickness of the film can be precisely modulated by the ink concentration and spin coating parameters, which typically requires sophisticated synthetic control in vapour-based CVD synthesis of 2D crystals[24,25,44]. For example, we have

https://doi.org/10.1038/s41928-025-01338-w

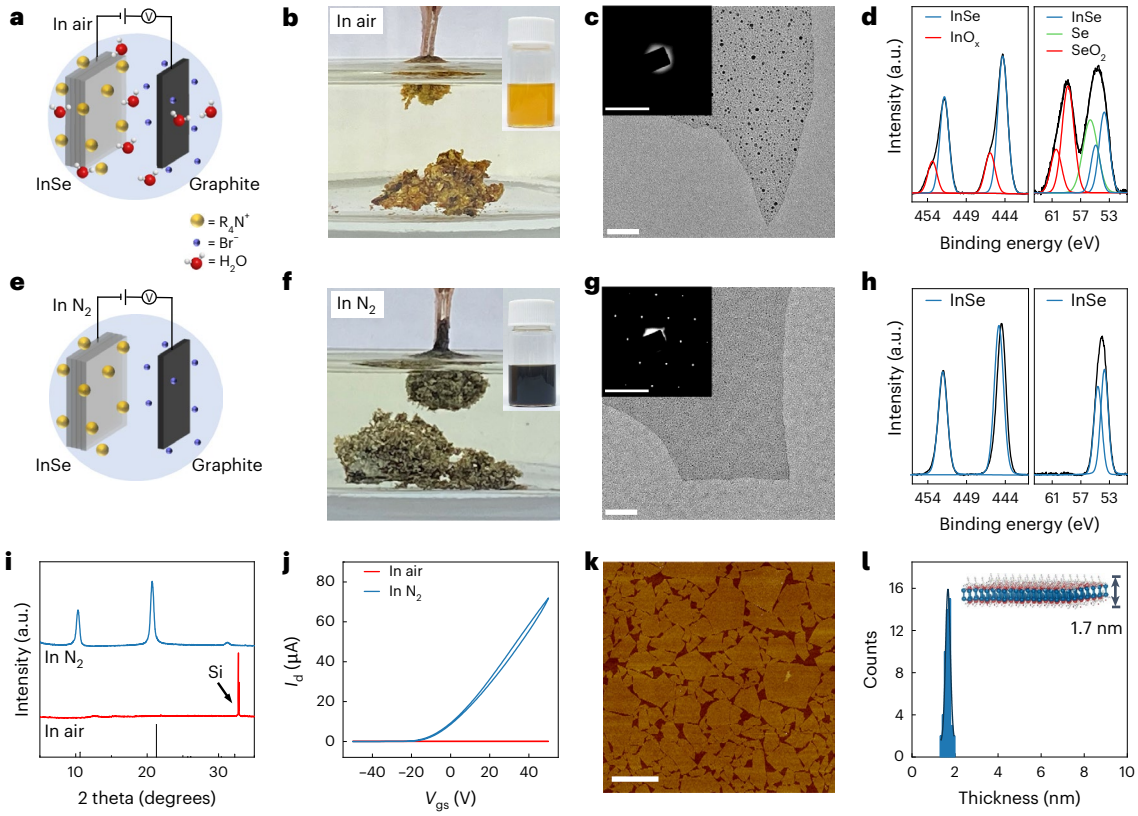

Fig. 1 | Understanding the effect of moisture in the electrochemical molecular intercalation and exfoliation of InSe crystal. a, Schematic illustration of the electrochemical molecular intercalation of InSe bulk crystal in air with the presence of dissolved moisture and oxygen in solvent. **b**, A thin piece of InSe crystal intercalated in air. **c**, TEM image of the InSe monolayer intercalated and exfoliated in air, showing a large number of impurity particles due to material oxidation. Inset is the electron diffraction pattern of the monolayer that signifies the destruction of crystal lattice. Scale bars are 100 nm for TEM image and 5 1/nm for electron diffraction pattern. **d**, XPS spectra of InSe monolayers in air, showing the new peaks for InO_x, Se and SeO_2 due to the material oxidation. **e**, Schematic illustration of the electrochemical molecular intercalation of InSe bulk crystal in nitrogen with dry solvent. **f**, A thin piece of InSe crystal intercalated in nitrogen. **g**, TEM image and electron diffraction pattern of the InSe monolayer intercalated and exfoliated in nitrogen, suggesting an oxidation-free crystal structure. Scale bars are 100 nm for TEM image and 5 1/nm for electron diffraction pattern. **h**, XPS spectra of InSe monolayers in nitrogen, showing that no sign of material oxidation was detected in the XPS measurement. **i**, XRD patterns of InSe monolayers intercalated and exfoliated in air and nitrogen, respectively. The vertical lines indicate the diffraction peaks of pristine InSe crystal, which disappear when processed in air. **j**, Electrical characterizations of InSe monolayers intercalated and exfoliated in air and nitrogen, respectively. The InSe exfoliated in nitrogen exhibits the pristine n-type transport behaviour while the InSe exfoliated in air is not conductive. **k**, AFM image of InSe monolayers deposited on SiO_2/Si substrate, showing nearly identical colour contrast and thickness among all monolayers. Scale bar is 2 μm. **l**, Statistical thickness analysis that suggests a narrow thickness distribution of InSe monolayers. Inset is the structure model of the InSe monolayer with ammonium molecules on surface.

obtained THAB/InSe thin films with thickness of 7.0 to 47 nm (Fig. 2b and Supplementary Fig. 9), corresponding to InSe crystals with thicknesses of 3.5 to 25 nm after thermal annealing at 300 °C (Fig. 2c). By simply optimizing the ink concentration, InSe thin films with thicknesses of 0.8 to 5.0 nm (that is, corresponding to one- to six-layer crystals) were spin coated for one to six times, respectively (two red curves in Fig. 2c). For all these films, a good linear relationship between the film thickness and spin coating cycle number was observed. The XRD pattern of the assembled InSe films suggests an organic–inorganic THAB/InSe hybrid superlattice structure ($d \approx 1.6$ nm) (Fig. 2d), matching the thickness of individual nanosheet in AFM. The emergence of only (00l) peaks in the XRD pattern suggests highly ordered and oriented nanosheets stacking in the film. After thermal annealing at more than 200 °C to eliminate the organic molecules, the THAB/InSe superlattice structure collapsed into pure-phase InSe crystals ($d \approx 0.8$ nm), matching with the film thickness reduction by ~50% observed in AFM results (Fig. 2c). XPS analyses indicate the retained InSe structure after thermal annealing (Supplementary Fig. 10). By contrast, the THAB/InSe nanosheets exfoliated in air could not be converted to InSe crystal after thermal annealing due to the damaged crystal structure (Fig. 1i).

In cross-sectional TEM analyses, the close and conformal stacking between monolayer nanosheets was observed in the as-deposited THAB/InSe thin film (Fig. 2e). For the as-assembled THAB/InSe superlattice thin film, the vertical lattice periodicity is ~1.6 nm (Fig. 2f,g and Supplementary Fig. 11a), matching values obtained in AFM and XRD analyses. After thermal annealing, the thickness of film was reduced to ~25 nm with the chemical conversion from THAB/InSe superlattice to pure InSe crystal (Fig. 2h). The chemically converted InSe thin film has a lattice periodicity of ~0.8 nm, which coincides with the intrinsic interlayer distance in pristine crystal (Fig. 2i,j and Supplementary Fig. 11b). Here both the THAB/InSe superlattice and the converted InSe films are uniform in thickness, compact and free of voids in microscopic level. Specifically, the clean and conformal van der Waals contact between InSe monolayers resembles the pristine bulk crystal, representing high material quality in the assembled thin films. Raman spectroscopical analysis of the assembled InSe thin film also indicates a high crystal quality comparable to the bulk crystal (Supplementary Fig. 12). AFM analysis reveals smooth film surfaces with a small roughness of ~2 nm (Supplementary Fig. 13). With these results, we have demonstrated the wafer-scale assembly of high-quality uniform and compact InSe thin films with precisely modulated thickness using the solution-based processing method.

https://doi.org/10.1038/s41928-025-01338-w

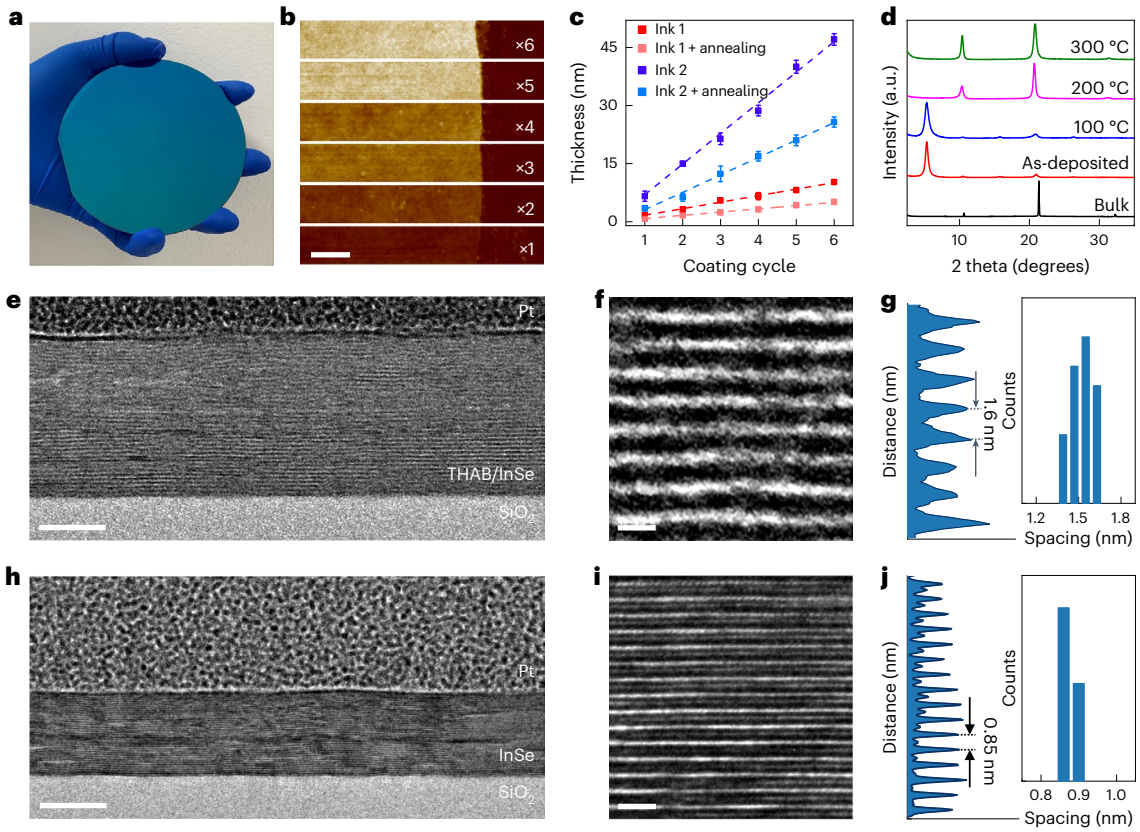

Fig. 2 | Solution-processable wafer-scale InSe thin film using the monolayer ink. a, Photograph of the wafer-scale InSe thin film deposited on 4-inch SiO_2/Si substrate. **b**, AFM images of various InSe thin films with tunable thickness by spin coating one to six times. Scale bar is 2 µm. **c**, The linear relationship between the thickness of deposited thin films and the number of coating cycles, demonstrating a fine control of thickness. Data points represent mean values of thickness. The error bars are standard deviations based on the differences between five samples. **d**, XRD patterns of the pristine bulk crystal and the assembled thin films annealed at different temperatures. **e**,**f**, Cross-sectional TEM images of the THAB/InSe thin film on SiO_2/Si substrate. Scale bars are 20 nm (**e**) and 2 nm (**f**). **g**, Statistical distribution of THAB/InSe superlattice periodicity in the TEM image in **f**. **h**,**i**, Cross-sectional TEM images of the pure InSe thin film converted from THAB/InSe superlattice in **e**. Scale bars are 20 nm (**h**) and 2 nm (**i**). **j**, Statistical distribution of InSe crystal periodicity in the TEM image in **i**.

Electrical characteristics of the solution-processed InSe thin films

Electrical characterizations of the assembled InSe thin films have further revealed the preserved semiconducting characteristics. The field-effect transistors were fabricated on SiO_2/Si substrate by depositing electrodes through a metal shadow mask (Fig. 3a). The dielectric layer is SiO_2 with a thickness of ~200 nm (Supplementary Fig. 14) and the typical channel length and width is 300 and 300 µm and 200 and 200 µm. Transistors of other channel length and width values such as 20/180 µm were fabricated by a standard photolithography process (Supplementary Fig. 15a–c). To define an accurate channel length and width and suppress the gate leakage current, the transistor was isolated from the other area of the film by scratching off the material outside the channel area. Here we report the transistor performance following the previously established guidance[45]. The as-assembled THAB/InSe superlattice thin film is not electrically conductive due to the insulating ammonium molecules. After thermal annealing, the THAB/InSe superlattice structure can be converted to pure InSe crystal and the n-type transport behaviour emerges (Fig. 3b). Although XRD patterns suggest the recovery of pure InSe lattice after thermal annealing at over 200 °C, the highest current was observed in the film annealed at 300 °C. Further increasing the annealing temperature results in a crystal phase change to other material and thus the lower current (Supplementary Fig. 16). For thicker films, the current in transistor grows higher (Fig. 3c,d) for the increased amount of materials and conducting paths along the vertical direction. The current on/off ratio gradually decreases from ~10^7 to ~10 along with the growing I_{off} (Supplementary Fig. 17a,b). The weaker drain current modulation and smaller on/off ratio are mostly due to the screening of gate electric field and limited gate modulation depth of SiO_2 dielectric[46]. Meanwhile, V_{th} shifts to negative values in thicker films (Supplementary Fig. 17c), as commonly seen in many 2D semiconductor[20,37]. Similar to the trend of the current level, the highest carrier mobility was observed in the thin film annealed at 300 °C (Fig. 3e and Supplementary Fig. 18). Using the InSe thin film with a thickness of ~17 nm (annealed at 300 °C), the fabricated transistor on standard SiO_2 dielectric delivered a carrier mobility of ~95 $cm^2 V^{-1} s^{-1}$ and current on/off ratio of 10^7. The field-effect mobility (μ_{FE}) values were calculated in the linear region following the equation $\mu_{FE} = L_{ch} \times g_m/(W_{ch} \times C_{ox} \times V_{ds})$, in which L_{ch} and W_{ch} are the channel length and width, g_m is the measured transconductance, C_{ox} is the capacitance of the gate oxide dielectric and V_{ds} is the drain-source voltage of the transistor. The carrier mobility eventually saturates at ~120 $cm^2 V^{-1} s^{-1}$ for film thickness over 30 nm despite the lower current on/off ratio (Fig. 3f).

Using the film with a thickness of ~25 nm as a representative example, we measured the I_d–V_{ds} output curves of the transistor under various gate bias (Fig. 3g). At small voltage values, the I_d–V_{ds} curves are linear, which thus suggests an Ohmic contact between the metal electrodes and semiconductor. Among multiple devices tested on the same film, all mobility values fall in the range of 100–120 $cm^2 V^{-1} s^{-1}$ and the current on/off ratios are ~10^5 (Fig. 3h). The narrow distribution of mobility values confirms the high material and device uniformity. The detailed transistor performance of different InSe thicknesses, including mobility, on/off ratio, SS value and so on, are summarized for a clear and transparent comparison (Supplementary Table 1). The

https://doi.org/10.1038/s41928-025-01338-w

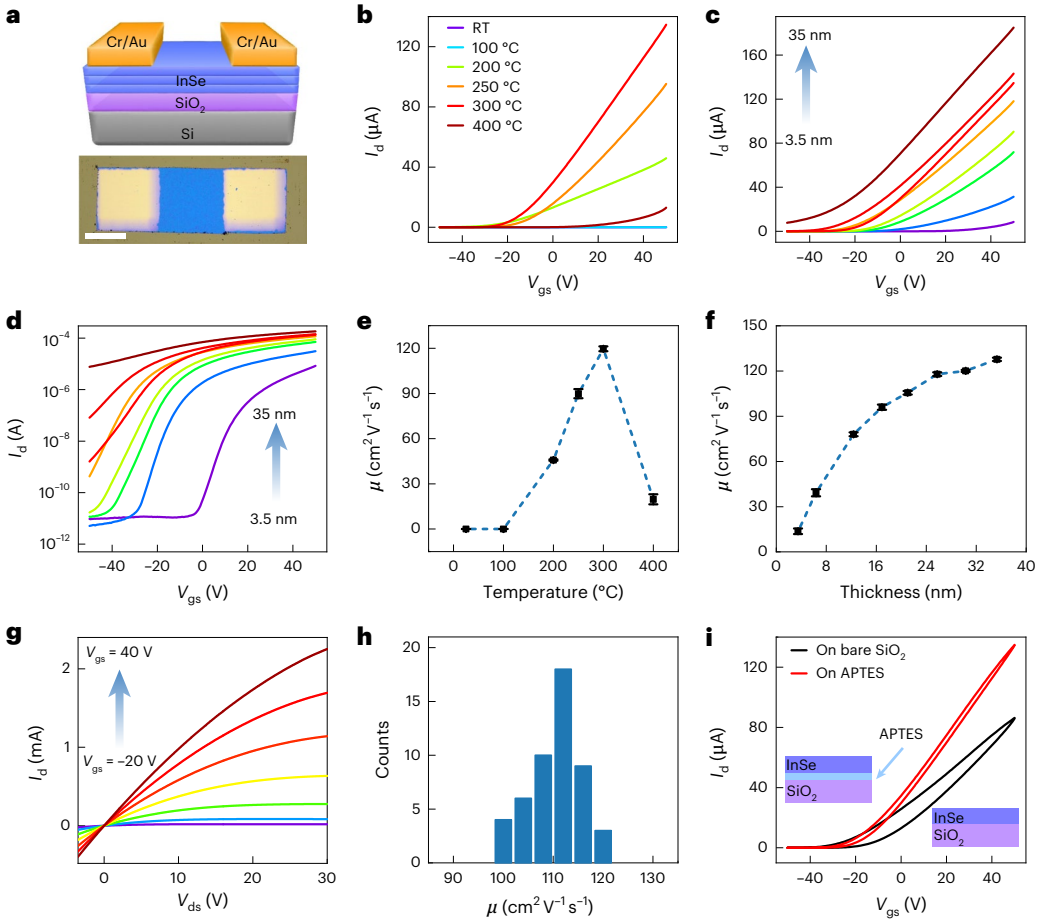

Fig. 3 | Electrical characterizations of the InSe thin films. a, Schematic illustration and optical image of the bottom-gate/top-contact transistor with InSe semiconductor channel. Scale bar is 200 μm. **b**, I_d–V_{gs} transfer curves InSe thin films annealed at different temperature up to 400 °C. V_{ds} = 1 V. L/W = 1. The gate voltage sweeps from 50 to −50 V. RT, room temperature. **c**,**d**, I_d–V_{gs} transfer curves of InSe thin films annealed at 300 °C of various thickness from 3.5, 6.4, 12, 17, 21, 25, 30 to 35 nm, which are plotted in both linear (**c**) and logarithm (**d**) scales. V_{ds} = 1 V. L/W = 1. **e**,**f**, The carrier mobility of InSe thin films annealed at different temperatures (**e**) and at different thicknesses (**f**). The film thickness in **e** is 25 nm. Data points represent mean values of the carrier mobility. The error bars are standard deviations based on the differences between three devices. **g**, I_d–V_{ds} output curves of the InSe thin film with thickness of 25 nm and annealed at 300 °C, under gate bias from −20 to 40 V. **h**, Statistical distribution of mobility values measured from 50 individual InSe transistors on the same thin film with thickness of 25 nm and annealed at 300 °C. **i**, Forwards and backwards scan in I_d–V_{gs} transfer curves of InSe assembled on bare SiO_2/Si substrate and that on substrate functionalized with a SAM of APTES molecules. V_{ds} = 1 V. L/W = 1.

transistors fabricated by the photolithography process show consistent current and mobility values to those prepared by shadow mask (Supplementary Fig. 15d–i). In addition, logic gates such as inverter, AND, NOR and NAND were fabricated and the basic logic operation was demonstrated (Supplementary Fig. 19). Last, the carrier mobility extracted from field-effect transistors was also validated by Hall effect measurement (Supplementary Fig. 20).

These mobility values are higher than the previous large-scale InSe thin films (thickness ~0.8–40 nm) produced from either vacuum-based PLD[36,37], CVD[38,47,48] or solution-based exfoliation by one or two orders of magnitude[8,39,40] (Supplementary Table 1). For example, a recent study reported the first continuous 2-inch wafer-scale InSe thin film (thickness ~5 nm) with a carrier mobility of ~4.5 $cm^2 V^{-1} s^{-1}$ and on/off ratio of ~10^6 synthesized by metal-organic CVD[38], which differs from previous discrete individual crystalline flakes or non-uniform thin films by regular CVD methods[37,47–49]. Other reports on the mobility and on/off ratio of large-area InSe thin films include ~0.2 $cm^2 V^{-1} s^{-1}$ and ~10^4 (15-nm-thick, PLD)[36], ~70 $cm^2 V^{-1} s^{-1}$ and <10^2 (20-nm-thick, PLD)[37], ~2 $cm^2 V^{-1} s^{-1}$ and ~10^5 (30-nm-thick, solution-based)[39] and <0.1 $cm^2 V^{-1} s^{-1}$ and <10 (515-nm-thick, solution-based)[40]. An ideal comparison of mobility should be made between InSe crystals of the same thickness. However, due to the limited reports on the growth of large-scale InSe thin films, the mobility values of InSe thin films in this work are not compared with other InSe of the exactly same thickness. Additionally, the mobility here is even comparable to the state-of-the-art performance of CVD-grown wafer-scale 2D MoS_2 semiconductor thin films (average μ of ~100–120 $cm^2 V^{-1} s^{-1}$ and up to ~190 $cm^2 V^{-1} s^{-1}$ for monolayer to trilayer MoS_2 of 1- or 2-inch size) (Supplementary Fig. 21)[24–27]. It should be noted that these wafer-scale MoS_2 are much thinner than the InSe thin films reported in this work. In the next step, the integration of high-k dielectrics such as HfO_2 and sodium-embedded Al_2O_3 may further boost the transistor performance[23,50].

Another unique merit of the fabricated InSe transistors is the small current hysteresis in the I_d–V_{gs} transfer curves. For the forwards and backwards I_d–V_{gs} scans, the InSe transistors using conventional SiO_2/Si back gate exhibit similar on-current, threshold voltage, carrier mobility and SS value (Fig. 3i and the next section). This has been previously challenging for InSe transistors on SiO_2/Si substrate due to the interfacial trapping states or hydroxyl group on the oxide surface, which was found to reduce the measured carrier mobility and induce current hysteresis[29,33,51]. Usually, switching the substrate to hexagonal boron nitride (h-BN) or polymer dielectric can mitigate the hysteresis issue and improve the current and mobility but requires additional manufacturing process[29,33,52]. In this case, we adopted a facile and robust

https://doi.org/10.1038/s41928-025-01338-w

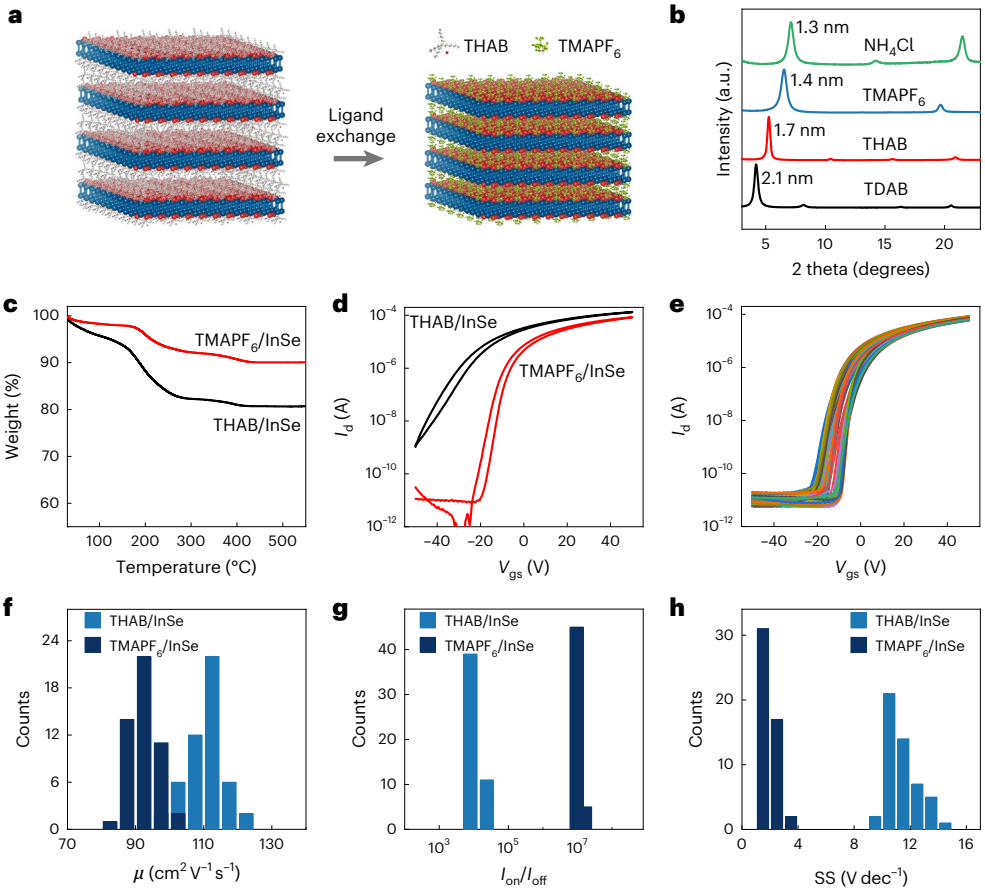

Fig. 4 | Tuning the electrical performance with ligand exchange process. **a**, Schematic illustration of ligand exchange process on the assembled thin films. **b**, XRD patterns of THAB/InSe thin films exchanged with different molecules and inorganic salts, showing structural periodicity from 1.3 to 2.1 nm. **c**, TGA analyses of THAB/InSe and $TMAPF_6$/InSe superlattices that show different content of organic molecules. **d**, I_d–V_{gs} transfer curves of InSe thin films converted from THAB/InSe and $TMAPF_6$/InSe superlattices, respectively. V_{ds} = 1 V. L/W = 1. **e**, 50 individual I_d–V_{gs} transfer curves measured on the same InSe thin film converted from $TMAPF_6$/InSe superlattices, showing high material and device uniformity. V_{ds} = 1 V. L/W = 1. The gate voltage sweeps from 50 V to −50 V. **f**–**h**, Comparison of device characteristics including carrier mobility (**f**), current on/off ratio (**g**) and SS value (**h**) between InSe thin films converted from THAB/InSe and $TMAPF_6$/InSe superlattices, respectively.

substrate functionalization strategy by growing self-assembled monolayer (SAM) of (3-aminopropyl)triethoxysilane (APTES) on the SiO_2/Si substrate surface. With the APTES functionalization, the InSe transistors exhibit higher current and smaller hysteresis than that on bare SiO_2/Si substrate (Fig. 3i and Supplementary Fig. 22). For example, the ΔV between forwards and backwards scans in a transfer curve of InSe thin films (at I_d = 1 μA) decreased from 14.8 V to 4.2 V after the substrate was functionalized with APTES layer. Later, we will show that the small current hysteresis was also observed in InSe thin films after the ligand exchange process. The functionalization with close-packing SAM prevents the direct contact between InSe and the underlying SiO_2 surface and thus screens interfacial trapping states and hydroxyl group, which is important for realizing InSe transistors with greatly reduced current hysteresis and improved device reliability.

Device performance after ligand exchange

Versatile organic–inorganic and inorganic–inorganic hybrid superlattice materials were constructed by replacing the THAB with other molecules of distinct chemical composition and structures (Fig. 4a). Tetradecylammonium bromide (TDAB) expanded the interlayer distance from 1.7 nm in THAB/InSe to 2.1 nm in TDAB/InSe (Fig. 4b). Substituting the THAB with smaller ligands such as tetramethylammonium hexafluorophosphate ($TMAPF_6$) and inorganic NH_4Cl through a ligand exchange process results in the lattice shrink to ~1.4 and 1.3 nm, respectively. Other hybrid superlattice structures consisting of different ammonium molecules were also constructed (Supplementary Fig. 23). In addition, the ligand exchange process can also be performed in the liquid phase to obtain the colloidal solution of dispersed InSe nanosheets that are capped with other molecules such as $TMAPF_6$. The XRD pattern confirms the successful ligand exchange in the liquid phase (Supplementary Fig. 24). Versatile organic–inorganic and inorganic–inorganic hybrid superlattice materials may be constructed with distinct physical properties.

As a proof of concept, we investigated the superlattice thin film exchanged with $TMAPF_6$. In specific, the deposited THAB/InSe thin film was immersed in the solution containing different salts for ligand exchange (Methods). Ascribing to the smaller size of the TMA^+ cation compared with THA^+ cation, the organic content in the superlattice is reduced by ~50% (by weight) as revealed by thermogravimetric analysis (TGA) (Fig. 4c). The $TMAPF_6$/InSe superlattice, similar to THAB/InSe, can be chemically converted to pure InSe crystal after thermal annealing (Supplementary Fig. 25). However, these two types of InSe thin film derived from THAB/InSe and $TMAPF_6$/InSe superlattices display distinct electrical characteristics. For example, a sharp decrease of the SS value from 11.2 to 1.8 V dec^{-1} was observed in the InSe thin films derived from $TMAPF_6$/InSe compared with the counterparts from THAB/InSe (Fig. 4d). This SS value is superior to previous solution-processable 2D semiconductor thin films gated with conventional thermal oxide on

https://doi.org/10.1038/s41928-025-01338-w

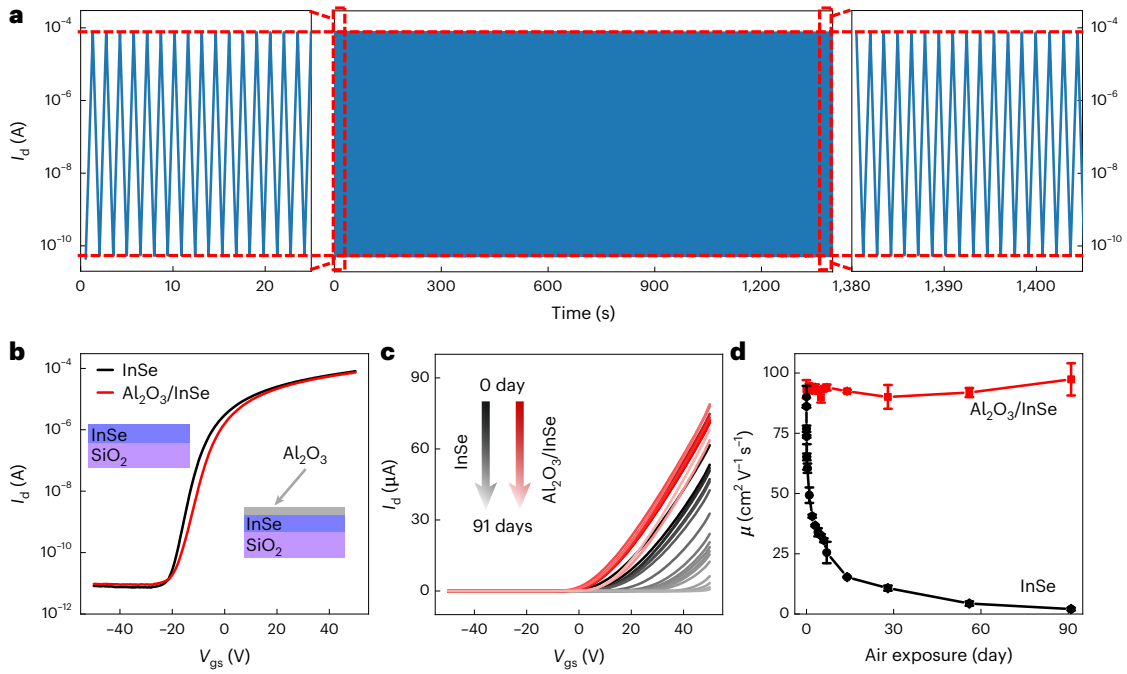

Fig. 5 | Device stability of the InSe transistors. a, Continuous on/off switching test for 2,000 cycles (V_{gs} ± 50 V, V_{ds} = 1 V) of one representative transistor with InSe converted from $TMAPF_6$/InSe. **b**, I_d–V_{gs} transfer curves of InSe transistor before and after the encapsulation of 10-nm-thick Al_2O_3 layer, respectively. V_{ds} = 1 V. L/W = 1. The gate voltage sweeps from 50 to −50 V. **c**, Device stability of InSe (without encapsulation, black curves) and Al_2O_3/InSe (with encapsulation, red curves), after exposure to ambient air for 3 months. The device was measured at 0 h, 0.5 h, 1 h, 2 h, 3 h, 4 h, 8 h, 1 day, 2 days, 3 days, 4 days, 5 days, 6 days, 7 days, 14 days, 28 days, 56 days and 91 days. V_{ds} = 1 V. L/W = 1. **d**, Stability test of carrier mobility of InSe and Al_2O_3/InSe in **c**. The encapsulated Al_2O_3/InSe transistor exhibits nearly unchanged carrier mobility after exposure to air for 3 months while the bare InSe transistor shows a much quicker performance decay. Data points represent mean values of the carrier mobility. The error bars are standard deviations based on the differences between three devices.

silicon (~5–10 V dec^{-1} in MoS_2 and In_2Se_3)[2,39,43], indicating a high-quality 2D semiconductor thin film with reduced number of impurities, trapping states and chemical disorders. Potential trace organic residues that remain in the film and dielectric–semiconductor interface after the thermal conversion from hybrid superlattice to InSe might play a role here. Due to the lower content of organic molecules in $TMAPF_6$/InSe than that in THAB/InSe, these trace organic residues after thermal annealing may be further suppressed, which enables smaller SS values. To date, the exact origin remains elusive, which thus requires further detailed investigations on the doping effect and trace organic residues in the InSe thin films and interfaces using other advanced characterization tools. In the meantime, the current on/off ratio of the transistor also increased from 10^5 to 10^7 benefiting from the improved SS value and lower off current. A small current hysteresis was observed in the I_d–V_{gs} transfer curve of the InSe transistor enabled by the APTES functionalization (Fig. 4d and Supplementary Fig. 26), in consistence with InSe converted from THAB/InSe. Similarly, the I_d–V_{ds} output curves confirm the high current level and Ohmic contact (Supplementary Fig. 27). Also, the ligand exchange can be carried out with other species or pure solvents (Supplementary Fig. 28).

To test the film and device uniformity after ligand exchange, we have measured the I_d–V_{gs} transfer curves of 50 individual transistors on the same film (Fig. 4e and Supplementary Fig. 29). A small device-to-device performance variation among these 50 transistors was obtained. The difference between the electrical characteristics of two types of InSe converted from THAB/InSe and $TMAPF_6$/InSe have been systematically investigated in terms of the statistical distribution of carrier mobility, on/off ratio and SS value (Fig. 4f–h). In an optimized device, we have obtained a carrier mobility of ~92 ± 10 $cm^2 V^{-1} s^{-1}$, on/off ratio of ~10^7 and SS of 1.8 V dec^{-1} with a small current hysteresis, which represent the best transistor characteristics among all types of synthetic InSe thin film, including both wafer-scale thin films and discrete individual flakes[8,36–39,47–49]. Furthermore, to validate the wafer-scale uniformity of the material and electrical performance in the spin-coated InSe thin film, we have carried out detailed analyses of the film thickness (Supplementary Figs. 30 and 31) and transistor behaviour (Supplementary Figs. 32 and 33). The consistent thickness, mobility values (100–110 $cm^2 V^{-1} s^{-1}$) and on/off ratio (~10^7) at 16 different locations across the entire 4-inch film demonstrate the viability of producing wafer-scale 2D semiconductor thin films using solution-processable ink materials.

Device stability is another key figure of merit for thin-film transistors in practical applications that has also been investigated for the assembled InSe thin film. The fabricated InSe thin-film transistors show stable on/off switching characteristics for 2,000 cycles (V_{gs} between −50 and 50 V) in which both on and off current remain nearly constant during the continuous on/off operation (Fig. 5a). After repeatedly sweeping V_{gs} within the range of −50 to 50 V (continuously from −50 to 50 V and then back to −50 V) for 100 cycles, the device exhibits small drift in the I_d–V_{gs} transfer characteristics with a slight increase in the on-current (Supplementary Fig. 34a). During the more intensive stress test by holding the device at on-state (by applying a constant gate bias of 50 V), only a small drift in the transfer curves were observed after 5,400 s. The device characteristics can restore the original state once the constant positive gate bias is removed, suggesting the full recovery of the material and device (Supplementary Fig. 34b).

Air-stable InSe thin-film transistors were achieved by the facile encapsulation of device with a protective oxide layer. First, the InSe thin-film transistor was encapsulated with a 10 nm-thick Al_2O_3 layer (deposited by atomic layer deposition, ALD)[34,35]. For 2D semiconductors such as MoS_2, the ALD process of growing Al_2O_3 layer is usually accompanied by chemical doping to the semiconductor and thus dramatic alteration in transistor performance[53,54]. However, the impact of ALD process on device characteristics of InSe thin film is much smaller

(Fig. 5b and Supplementary Fig. 35). We noticed that the original device characteristics such as on-current, mobility and on/off ratio were preserved after exposure to the oxygen and moisture in the ambient air for 3 months (Fig. 5c). By contrast, the thin-film transistor without oxide encapsulation exhibits a quick decay by ~45% in current and mobility during the first day of exposure and up to 95% decay after 3 months. We believe the encapsulation with the Al_2O_3 protection layer isolates the InSe film from oxygen and moisture and thus improves the device stability in ambient air[34]. Therefore, the device characteristics of the Al_2O_3/InSe transistor are well preserved after exposure to ambient air for 3 months, including mobility (~95 $cm^2 V^{-1} s^{-1}$), on-current (70 μA) and current on/off ratio (~10^7) (Fig. 5d and Supplementary Figs. 36 and 37). The air-stable and high-performance InSe thin-film transistors may push forward the application of these 2D semiconductor-based transistors and integrated devices in diverse practical technological areas.

Conclusions

We have reported the solution-processable assembly of InSe semiconducting thin films on 4-inch wafer substrates. Our approach is based on spin coating ink materials formulated with a colloidal solution of high-purity 2D monolayers. A wide range of organic and/or inorganic superlattice structures were constructed with distinct chemical compositions and structures, which can be converted to pure inorganic InSe by thermal annealing. High-quality InSe thin films with intimate and conformal van der Waals contact between monolayers were assembled with precisely controlled thicknesses and high uniformity. Our InSe thin-film transistors on standard SiO_2 dielectrics exhibit average carrier mobilities of 90–120 $cm^2 V^{-1} s^{-1}$, on/off ratios of up to 10^7 and small current hysteresis. The mobility values of our devices approach state-of-the-art CVD-grown MoS_2 thin films at the wafer scale (average mobilities of around 100–120 $cm^2 V^{-1} s^{-1}$, with values up to around 190 $cm^2 V^{-1} s^{-1}$). Furthermore, air-stable InSe transistors were created through oxide protection, and shown to remain nearly unchanged after exposure to ambient air for 3 months. Our approach could be of use in the scalable fabrication of large-area, high-performance and air-stable electronic devices at affordable cost.

Methods

Synthesis of InSe bulk crystals

In (99.99%, metal basis, Macklin) and Se (99.9%, metal basis, Aladdin) powders were flame-sealed in a quartz ampoule at a molar ratio of 1:1 under a reduced pressure of 3×10^{-3} Pa. The sealed quartz ampoule was horizontally placed in a tube furnace (MTI KJ GSL-1200X) for slow heating to 850 °C and held at this temperature for 72 h. It was then allowed to cool to room temperature following a slow cooling method. High-quality bulk InSe crystals with smooth and shining surface can be obtained.

Formulation of high-quality InSe monolayer ink material

The electrochemical molecular intercalation and exfoliation of InSe monolayer crystals were carried out following our established protocol[22]. To assemble an electrochemical cell, THAB (98%, TCI) was dissolved in acetonitrile (ACN, 99.8%, water content ≤10 ppm, Adamas) as the electrolyte with a concentration of 0.01 M. A piece of freshly cleaved InSe crystal, conductive graphite rod and silver ion electrode (optional) were used as cathode, anode and reference electrode, respectively. The intercalation reaction was conducted at −3.2 V for 2 h. The InSe crystal notably expanded in volume with the intercalation of organic molecules. Once the intercalation reaction was completed, the InSe was transferred to 15 ml of DMF (99.8%, water content ≤10 ppm, Adamas) for exfoliation by regular bath sonication for 5 min. Tuning the sonication time and power leads to nanosheets of various lateral size as discussed in the main text. The above operations were all carried out in a N_2-filled glovebox with oxygen and water level lower than 1 ppm. Also, the acetonitrile and DMF solvents were degassed with nitrogen and dried with molecular sieve to ensure a low level of oxygen and moisture before use. A dark colloidal solution of 2D nanosheets can be obtained after exfoliation. The appearance of any yellow component in the final solid indicates potential material oxidation. After exfoliation, the InSe monolayers dispersed in solution were centrifuged at 1,697*g* for 5 min and precipitates were discarded to remove any bulk impurities. Then the monolayer nanosheets were precipitated by centrifugation at 12,838*g* for 10 min. The monolayer nanosheets were then redispersed into the desired amount of DMF (for example, 1–2 ml) as the final ink solution.

Substrate treatment before film deposition

Before spin coating, the SiO_2/Si substrate was treated with CH_3OH/HCl (volume ratio of 1:1) for 30 min at room temperature for a hydrophilic surface. The SAM of APTES (99%, Sigma-Aldrich) was prepared on the SiO_2/Si substrate following the established vapour-based method (growth time ~30 min) to modify the surface condition. The functionalized substrate was baked on a hotplate (120 °C, 30 min) in the glovebox to eliminate superfluous and uncondensed free silane molecules.

InSe thin film assembly and ligand exchange

Additional centrifugation at 1,071*g* for 5 min to discard the precipitate was performed on the InSe ink solution before adjusting the final concentration. Ultraviolet-visible light optical absorption spectroscopy (U-3900 PC, Hitachi) was used to monitor the concentration of the ink solution. A typical ink solution shows absorption of 2.20 at λ = 340 nm. InSe thin film was prepared on pretreated SiO_2/Si substrate by spin coating ink solution at 2,000 rpm for 20 s for the first cycle and 2,500 rpm for 20 s for the following cycles. Between each coating cycle, the film was baked at 100 °C on a hotplate for 3 min. For a typical InSe thin film used for transistor fabrication, six cycles of spin coating were applied. The final thickness of thin film depends on the ink concentration, spin rate and coating cycles. For example, another recipe for spin coating thin film of similar thickness on the wafer scale is to use a concentrated ink solution (absorption of 5.00) for just one coating cycle. For the ligand exchange process in an N_2-filled glovebox, the prepared thin films on the substrate were immersed in the exchange solution for 2 h (maybe longer if necessary) at room temperature, including tetramethylammonium hexafluorophosphate ($TMAPF_6$, 98%, TCI) (0.1 M), cetyltrimethylammonium bromide (CTAB, 98%, TCI) (0.01 M) and other quaternary ammonium salts dissolved in acetonitrile (0.1 M) as well as NH_4Cl (99.5%, Aladdin) in DMF (0.01 M). Then, the films were rinsed with clean solvent for 10–30 s before being blown dry in the glovebox. The InSe thin films with or without ligand exchange process were annealed at 300 °C for 2 h on a hotplate in an N_2-filled glovebox for further device fabrications.

Device fabrications

For the fabrication of thin-film transistors, the InSe film was deposited on the 200 nm SiO_2/Si substrate. The CH_3OH/HCl and APTES treatment were both performed on the substrate before film deposition to achieve optimal device performance. The source and drain electrodes were deposited by thermally evaporating Cr/Au (20/50 nm) layers through a shadow mask. While transferring the sample from the glovebox to the evaporator, the InSe thin film was exposed to ambient air for a short period of 2–3 min. After evaporation, the sample was also exposed to air for another 3–5 min before transferring into the measurement chamber of the probe station. For the device capsulation, Al_2O_3 layer with a thickness of 10 nm was deposited on the top of transistors using standard ALD (SVT ALD-P-100B). Before electrical measurements, all transistors were patterned by scratching off the film outside the channel area to obtain an accurate channel length and width. A metal microprobe was used to rub the material surface until the underlying thin film was scratched off the hard substrate. This process is repeated multiple times to obtain an isolation area surrounding the transistor. The logic gate devices were fabricated

with a local bottom gate (photolithography, Cr/Au, 10/30 nm) and Al_2O_3 dielectric layer (30 nm thickness grown by ALD at 200 °C). The deposited InSe thin film was patterned by photolithography and dry etching with an argon-based plasma etching process (ULVAC NE-550). Finally, another photolithography, oxide etching and metallization (Cr/Au, 20/50 nm) process were performed to finish the interconnection of electrodes.

Characterizations

The characterizations of the chemical composition and structure of InSe monolayers and thin films were performed with XRD (Bruker D8 Advance), SEM (Hitachi SU-8010), TEM (JEM-2100F, acceleration voltage, 300 kV), AFM (Bruker Dimension Icon scanning probe microscope), TGA (TA Instruments Q5000IR), Raman spectroscopy (Horiba LabRAM HR Evolution) and XPS (ESCALAB Xi). The electrical measurements of the transistors were performed with Keysight 2912B and B1500 measurement units in a Lakeshore vacuum probe station. During the measurement of the devices, the chamber was maintained in dark condition and vacuum with pressure below 10^{-1} Pa.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

References

1. Kelly, A. G. et al. All-printed thin-film transistors from networks of liquid-exfoliated nanosheets. *Science* **356**, 69–73 (2017).
2. Lin, Z. et al. Solution-processable 2D semiconductors for high-performance large-area electronics. *Nature* **562**, 254–258 (2018).
3. Carey, T. et al. Fully inkjet-printed two-dimensional material field-effect heterojunctions for wearable and textile electronics. *Nat. Commun.* **8**, 1202 (2017).
4. Zou, T. & Noh, Y.-Y. Solution-processed 2D transition metal dichalcogenides: materials to CMOS electronics. *Acc. Mater. Res.* **4**, 548–559 (2023).
5. Lin, Z., Huang, Y. & Duan, X. Van der Waals thin-film electronics. *Nat. Electron.* **2**, 378–388 (2019).
6. Kim, J. et al. Revisiting solution-based processing of van der Waals layered materials for electronics. *ACS Mater. Au* **2**, 382–393 (2022).
7. Kang, J., Sangwan, V., Wood, J. & Hersam, M. Solution-based processing of monodisperse two-dimensional nanomaterials. *Acc. Chem. Res.* **50**, 943–951 (2017).
8. Kang, J. et al. Solution-based processing of optoelectronically active indium selenide. *Adv. Mater.* **30**, 1802990 (2018).
9. Kim, J. et al. All-solution-processed van der Waals heterostructures for wafer-scale electronics. *Adv. Mater.* **34**, 2106110 (2022).
10. Zou, T. et al. High-performance solution-processed 2D p-type WSe_2 transistors and circuits through molecular doping. *Adv. Mater.* **35**, 2208934 (2023).
11. Li, P. et al. Flexible photodetectors based on all-solution-processed cu electrodes and InSe nanoflakes with high stabilities. *Adv. Funct. Mater.* **32**, 2108261 (2022).
12. Jeong, S. et al. Tandem intercalation strategy for single-layer nanosheets as an effective alternative to conventional exfoliation processes. *Nat. Commun.* **6**, 5763 (2015).
13. Kelly, A. G., O'Suilleabhain, D., Gabbett, C. & Coleman, J. N. The electrical conductivity of solution-processed nanosheet networks. *Nat. Rev. Mater.* **7**, 217–234 (2022).
14. Liu, Z. et al. General bottom-up colloidal synthesis of nano-monolayer transition-metal dichalcogenides with high 1T′-phase purity. *J. Am. Chem. Soc.* **144**, 4863–4873 (2022).
15. Pinilla, S., Coelho, J., Li, K., Liu, J. & Nicolosi, V. Two-dimensional material inks. *Nat. Rev. Mater.* **7**, 717–735 (2022).
16. Shen, J. et al. Liquid phase exfoliation of two-dimensional materials by directly probing and matching surface tension components. *Nano Lett.* **15**, 5449–5454 (2015).
17. Yang, R. et al. High-yield production of mono- or few-layer transition metal dichalcogenide nanosheets by an electrochemical lithium ion intercalation-based exfoliation method. *Nat. Protoc.* **17**, 358–377 (2022).
18. Zeng, Z. et al. Single-layer semiconducting nanosheets: high-yield preparation and device fabrication. *Angew. Chem. Int. Ed. Engl.* **50**, 11093–11097 (2011).
19. Dai, Y., He, Q., Huang, Y., Duan, X. & Lin, Z. Solution-processable and printable two-dimensional transition metal dichalcogenide inks. *Chem. Rev.* **124**, 5795–5845 (2024).
20. Xue, J. et al. Solution-processable assembly of 2D semiconductor thin films and superlattices with photoluminescent monolayer inks. *Chem* **10**, 1471–1484 (2024).
21. Wang, S. et al. A library of 2D electronic material inks synthesized by liquid-metal-assisted intercalation of crystal powders. *Nat. Commun.* **15**, 6388 (2024).
22. Wang, S. et al. Electrochemical molecular intercalation and exfoliation of solution-processable two-dimensional crystals. *Nat. Protoc.* **18**, 2814–2837 (2023).
23. Kwon, Y. A. et al. Wafer-scale transistor arrays fabricated using slot-die printing of molybdenum disulfide and sodium-embedded alumina. *Nat. Electron.* **6**, 443–450 (2023).
24. Li, T. et al. Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* **16**, 1201–1207 (2021).
25. Liu, L. et al. Uniform nucleation and epitaxy of bilayer molybdenum disulfide on sapphire. *Nature* **605**, 69–75 (2022).
26. Li, L. et al. Epitaxy of wafer-scale single-crystal MoS_2 monolayer via buffer layer control. *Nat. Commun.* **15**, 1825 (2024).
27. Qin, B. et al. Interfacial epitaxy of multilayer rhombohedral transition-metal dichalcogenide single crystals. *Science* **385**, 99–104 (2024).
28. Bandurin, D. A. et al. High electron mobility, quantum hall effect and anomalous optical response in atomically thin InSe. *Nat. Nanotechnol.* **12**, 223–227 (2017).
29. Jiang, J. et al. Stable InSe transistors with high-field effect mobility for reliable nerve signal sensing. *NPJ 2D Mater. Appl.* **3**, 29 (2019).
30. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).
31. Wang, F. et al. Piezopotential gated two-dimensional InSe field-effect transistor for designing a pressure sensor based on piezotronic effect. *Nano Energy* **70**, 104457 (2020).
32. Wang, Y. et al. Reduction of the ambient effect in multilayer InSe transistors and a strategy toward stable 2D-based optoelectronic applications. *Nanoscale* **12**, 18356–18362 (2020).
33. Feng, W., Zheng, W., Cao, W. & Hu, P. Back gated multilayer InSe transistors with enhanced carrier mobilities via the suppression of carrier scattering from a dielectric interface. *Adv. Mater.* **26**, 6587–6593 (2014).
34. Wells, S. A. et al. Suppressing ambient degradation of exfoliated InSe nanosheet devices via seeded atomic layer deposition encapsulation. *Nano Lett.* **18**, 7876–7882 (2018).
35. Ho, P.-H. et al. High-mobility InSe transistors: the role of surface oxides. *ACS Nano* **11**, 7362–7370 (2017).
36. Bergeron, H. et al. Large-area optoelectronic-grade InSe thin films via controlled phase evolution. *Appl. Phys. Rev.* **7**, 041402 (2020).
37. Yang, Z. et al. Wafer-scale synthesis of high-quality semiconducting two-dimensional layered InSe with broadband photoresponse. *ACS Nano* **11**, 4225–4236 (2017).

38. Song, S. et al. Wafer-scale growth of two-dimensional, phase-pure InSe. *Matter* **6**, 3483–3498 (2023).
39. Hao, Q. et al. Surface-modified ultrathin InSe nanosheets with enhanced stability and photoluminescence for high-performance optoelectronics. *ACS Nano* **14**, 11373–11382 (2020).
40. Curreli, N. et al. Liquid phase exfoliated indium selenide based highly sensitive photodetectors. *Adv. Funct. Mater.* **30**, 1908427 (2020).
41. Shi, L. et al. Oxidation mechanism and protection strategy of ultrathin indium selenide: insight from theory. *J. Phys. Chem. Lett.* **8**, 4368–4373 (2017).
42. D'Olimpio, G. et al. Enhanced electrocatalytic activity in GaSe and InSe nanosheets: the role of surface oxides. *Adv. Funct. Mater.* **30**, 2005466 (2020).
43. Lin, Z. et al. High-yield exfoliation of 2D semiconductor monolayers and reassembly of organic/inorganic artificial superlattices. *Chem* **7**, 1887–1902 (2021).
44. Hwangbo, S., Hu, L., Hoang, A. T., Choi, J. Y. & Ahn, J.-H. Wafer-scale monolithic integration of full-colour micro-LED display using MoS_2 transistor. *Nat. Nanotechnol.* **17**, 500–506 (2022).
45. Cheng, Z. et al. How to report and benchmark emerging field-effect transistors. *Nat. Electron.* **5**, 416–423 (2022).
46. Li, L. et al. Black phosphorus field-effect transistors. *Nat. Nanotechnol.* **9**, 372–377 (2014).
47. Chang, H.-C. et al. Synthesis of large-area InSe monolayers by chemical vapor deposition. *Small* **14**, 1802351 (2018).
48. Hu, Y. et al. Temperature-dependent growth of few layer β-InSe and α-In_2Se_3 single crystals for optoelectronic device. *Semicond. Sci. Technol.* **33**, 125002 (2018).
49. Zhou, J. et al. InSe monolayer: synthesis, structure and ultra-high second-harmonic generation. *2D Mater.* **5**, 025019 (2018).
50. Kang, K. et al. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520**, 656–660 (2015).
51. Tsai, T.-H. et al. High-mobility InSe transistors: the nature of charge transport. *ACS Appl. Mater. Interfaces* **11**, 35969–35976 (2019).
52. Chen, X. et al. High-quality sandwiched black phosphorus heterostructure and its quantum oscillations. *Nat. Commun.* **6**, 7315 (2015).
53. Na, J. et al. Low-frequency noise in multilayer MoS_2 field-effect transistors: the effect of high-k passivation. *Nanoscale* **6**, 433–441 (2014).
54. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).

Acknowledgements

Z.L. acknowledges the financial support from National Natural Science Foundation of China (NSFC, grant no. 22275113), Beijing Natural Science Foundation (grant no. Z240025), Tsinghua University Dushi programme and startup fund. We also acknowledge R. Zong and C. Ma in Analysis Center at Tsinghua University for their support of TEM characterizations. We acknowledge the Cell Biology Facility affiliated with the Center of Biomedical Analysis, Tsinghua University, for technical assistance and equipment support with Hitachi H-7650.

Author contributions

Z.L. designed and supervised the research. Z.L. and J.H. developed the intercalation and exfoliation approach for InSe crystal and the strategy for film deposition and device fabrication. J.H. performed the experiments on the material synthesis, structure characterizations and device measurements. J.G. and J.X. assisted with the material preparation and structural characterizations. T.X., Y.D., S.W. and W.L. assisted with the crystal growth and material synthesis. Z.L. and J.H. cowrote the paper. All authors discussed the results and commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41928-025-01338-w.

Correspondence and requests for materials should be addressed to Zhaoyang Lin.

Peer review information *Nature Electronics* thanks Yong-Young Noh and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.